

REMARKS

Claims 4-11 and 13-20 are pending in the above-identified application. Claims 4-11 and 13 were rejected. With this amendment, claims 4 and 13 were amended and new claims 14-20 were added. Applicants maintain that no new matter has been added with this amendment. Accordingly, claims 4-11 and 13 are at issue in the above-identification application.

In the Office Action mailed May 12, 2003, claim 13 was rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. In response, claim 13 has been amended to use consistent nomenclature. It is submitted that this rejection has been overcome.

Claims 4-7, 11, and 13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Kudo et al.* (U.S. Patent No. 6,190,975 B1) in view of *Imai et al.* (U.S. Patent No. 5,847,419) and further in view of *Taylor et al.* (U.S. Patent No. 6,410,941 B1). Regarding claims 8 and 10, the Examiner states that *Kudo et al.* and *Imai et al.* and *Taylor et al.* together disclose the structure set forth in those claims.

Amended claim 4 recites a semiconductor device comprising a p-channel field effect region having a silicon-germanium compound layer formed on and in *direct contact* with a substrate. New claim 14 recites a semiconductor device comprising an n-channel field effect region having drain and source regions *formed in said silicon epitaxial layer* on said relax layer and *not in said relax layer*. New claim 17 recites a semiconductor device comprising a silicon-germanium compound layer in *direct contact* with a first layer and a silicon-germanium compound relax layer in *direct contact* with a second layer, wherein the first and second layers comprise a different material.

Kubo et al fails to fairly teach or suggest this structure. In contrast, it is clear that the

source/drain regions in *Kubo et al.* are not so confined, nor are the silicon-germanium layers in *Kubo et al.* so bounded. In contrast, in *Kubo et al.*, the NMOS source drain regions extend in to the layer 15n. Moreover, there is the addition of the layer 14p in the PMOS region, which is not present in the present claims. Accordingly, neither *Kubo et al.*, *Taylor et al.*, nor *Imai et al.*, either alone or in combination suggest or teach a device as claimed in claims 4, 14, and 17, nor any of the dependent claim 5-11, 13, 15, 16, and 18-20.

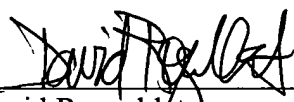
CONCLUSION

In view of the remarks set forth above, Applicant respectfully submits that the present invention is in condition for allowance. Early notification to such effect is earnestly solicited. Should the Examiner have any remaining issue, Applicant kindly requests that the Examiner contact the undersigned.

Respectfully submitted,

Dated: September 12, 2003

By:



David Rozenblat
Registration No. 47,044
SONNENSCHN NATH & ROSENTHAL LLP
P.O. Box 061080
Wacker Drive Station, Sears Tower
Chicago, Illinois 60606-1080
(312) 876-8000